Gyanmanjari Innovative University

Course Syllabus
Gyanmanjari Institute of Technology
Semester-6 (B.Tech.)

Subject: Computer Organization and Architecture-BETCE16328

Type of course: Professional Core and Professional Elective Courses

Prerequisite: Basic knowledge of Electronics

Rationale:

The Computer Organization and Architecture is a core subject that helps students understand the internal functioning of computer systems. It bridges the gap between hardware and software by explaining how instructions are processed, how memory is organized, and how data flows within a computer. This course equips students with the knowledge of processor architecture, instruction sets, memory hierarchy, and I/O systems, forming the foundation for advanced topics like operating systems, compilers, and embedded systems. Understanding COA is essential for system design, performance optimization, and effective programming at the low level.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks					Total Marks
				Theory Marks		Practical Marks		CA	
CI	T	P	C	ESE	MSE	V	P	ALA	
3	0	0	3	60	30	10	00	50	150

Legends: CI-Classroom Instructions; T – Tutorial; P - Practical; C – Credit; ESE - End Semester Examination; MSE- Mid Semester Examination; V – Viva; CA - Continuous Assessment; ALA- Active Learning Activities.

GYANMANJARI INNOVATIVE UNIVERSITY BHAVNAGAR

Course Content:

Sr. No	Course Content	Hrs.	% Weightage
1	**Introduction to Computer Architecture** Register transfer language, Bus and memory transfer, Arithmetic, logic and shift micro-operations. **Basic Computer Organization and Design** Computer registers, Computer instructions, Timing and control, Instruction cycle, Memory reference instructions, Input-Output and interrupt, complete computer description, Control Memory, Address sequencing, Microprogram example, Design of Control unit.	14	30%
2	**Assembly Language Programming** Introduction, Machine Language, Assembly Language Programming: Arithmetic and logic operations, looping constructs, Subroutines, I-O Programming.	06	12%
3	**Central Processing Unit** Introduction, General register organization, Stack organization, Instruction formats, addressing modes, Data transfer and manipulation, Program control, Reduced Instruction Set Computer (RISC), Complex Instruction Set Computer (CISC), Pipelining, Arithmetic pipelining, Instruction pipelining, RISC pipeline. **Computer Arithmetic** Binary Arithmetic, Add, Subtract, Multiply, Divide, Algorithms.	13	28%
4	**Input Output Organization** Input output interface, Asynchronous data transfer, Modes of transfer, Priority interrupt, Direct Memory access (DMA), Input output processor (IOP), CPU-IOP communication. **Memory Organization** Memory hierarchy, Main memory, Auxiliary Memory, Associative memory, Cache memory, Virtual Memory.	08	20%
5	**Muitiprocessors** Characteristics of Multiprocessors, Interconnection Structures, Inter-processor Arbitration, Inter-processor Communication and Synchronization, Cache Coherence, Shared Memory Multiprocessors.	04	10%

Continuous Assessment:

Sr. No	Active Learning Activities	Marks
1	**Micro-Operation Design Lab** Students will individually design micro-operations for a custom instruction set on simulation tools i.e. Logisim. They can use micro-operations like Register Transfer Micro-Operations, Arithmetic Micro-Operations, Logic Micro-Operations, Control Micro-Operations, Memory Transfer Micro-Operations, Input/Output Micro-Operations. After the completion of simulation, they have to prepare output of simulation document in PDF format and upload on GMIU web portal.	10
2	**Memory Matching Game** Students will individually create presentation of memory addresses, cache blocks, pages, and frame numbers. Match them correctly based on addressing scheme. After the completion of matching, they have to upload presentation on GMIU web portal.	10
3	**I/O Mechanism** Students will individually simulate how data flows in Programmed I/O, Interrupt I/O, and DMA on simulation tools i.e. Logisim. After the completion of simulation, they have to prepare output of simulation document in PDF format and upload on GMIU web portal.	10
4	**Design Your Own RISC CPU** Students will individually design a minimal RISC architecture. Sketch CPU block diagram and describe instruction format, data path, control logic in a single document. After the completion they have to prepare this document in PDF format and upload on GMIU web portal.	10
5	**Case Study** Students will individually pick a real CPU i.e. ARM Cortex, Intel i7, MIPS. They have to prepare detailed case study analysis on CPU. After the completion of case study they have to prepare the poster of this in PDF format and upload on GMIU web portal.	10
	Total	50

Suggested Specification table with Marks (Theory): 60

Distribution of Theory Marks (Revised Bloom's Taxonomy)						
Level	Remembrance (R)	Understanding (U)	Application (A)	Analyze (N)	Evaluate (E)	Create (C)
Weightage %	25%	32%	20%	20%	03%	-

Course Outcome:

After learning the course the students should be able to:	
CO1	Identify and explain the basic structure and functional units of a digital computer.
CO2	Write assembly language programs and identify the role and working of various functional units of a computer for executing an instruction.
CO3	Design processing unit using the concepts of ALU and control logic design.
CO4	Create circuits for interfacing memory and I/O with processor.
CO5	Comprehend the features and performance parameters of different types of computer architectures.

Instructional Method:

The course delivery method will depend upon the requirement of content and need of students. The teacher in addition to conventional teaching method by black board, may also use any of tools such as demonstration, role play, Quiz, brainstorming, MOOCs etc.

From the content 10% topics are suggested for flipped mode instruction.

Students will use supplementary resources such as online videos, NPTEL/SWAYAM videos, e-courses, Virtual Laboratory.

The internal evaluation will be done on the basis of Active Learning Assignment.

Practical/Viva examination will be conducted at the end of semester for evaluation of performance of students in laboratory.

Reference Books:

[1] M. Morris Mano, "Computer System Architecture", Pearson Education.

[2] Andrew S. Tanenbaum and Todd Austin, "Structured Computer Organization", Pearson Education.

[3] R.S.Gaonkar, "Microprocessor Architecture, Programming and Applications with 8085A", Penram International.

[4] Yale N. Patt, Sanjay J. Patel, "Introduction to Computing Systems" McGraw Hill.

[5] Douglas Hall, Microprocessors and Interfacing, Tata McGraw Hill.